# DANIEL LUSTIG

Research Scientist
NVIDIA Research
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## EDUCATION

2009 – 2015 **Princeton University**, Princeton, NJ
Ph.D. in Electrical Engineering, November 2015
M.A. in Electrical Engineering, September 2011
Advisor: Margaret Martonosi

2005 – 2009 **University of Pennsylvania**, Philadelphia, PA
B.S.E., *summa cum laude*, May 2009
Majors: Electrical Engineering, Mathematics

## PROFESSIONAL EXPERIENCE

Nov. 2015 – Present **NVIDIA Research**, Santa Clara, CA
Research Scientist, Architecture Research Group

Sep. 2009 – Nov. 2015 **Princeton University**, Princeton, NJ
Graduate Student, Dept. of Electrical Engineering
Advisor: Margaret Martonosi

Summer 2013, Summer 2012, Summer 2011 **Intel**, VSSAD Group, Hudson, MA
Graduate Technical Intern
Topic: Triggered Instructions accelerator
Supervisors: Joel Emer, Michael Pellauer, Angshuman Parashar

Fall 2010 **Intel**, Digital Enterprise Group, Hillsboro, OR
Graduate Technical Intern
Topic: prototyped a 10Gbps Ethernet TCP/IP+IPSec packet processor on a heterogeneous Xeon, Atom, and FPGA server platform
Supervisor: Ganapati Srinivasa

Summer 2008 – Summer 2009 **University of Pennsylvania,** mLAB, Philadelphia, PA
Research Assistant, Dept. of Electrical and Systems Engineering
Topic: using CUDA to develop AutoMatrix traffic simulation software
Advisor: Rahul Mangharam

## AWARDS AND HONORS

- CCICheck nominated for Best Paper at MICRO 2015 (one of three nominees)
- PipeCheck chosen as a IEEE Micro Top Pick of 2014
- PipeCheck nominated for Best Paper at MICRO 2014 (one of five nominees)

- Best in Session at SRC TECHCON 2014
- Intel PhD Fellowship, Fall 2013 – Spring 2014
- Triggered Instructions paper chosen as a IEEE Micro Top Pick of 2013
- Featured Inventor, Celebrate Princeton Invention 2012
- Francis Upton Fellowship, Princeton University, Fall 2009 – Present
- William L. Everitt Student Award of Excellence, University of Pennsylvania, Spring 2009
- Faculty Appreciation Award, University of Pennsylvania, Spring 2009
- Honorable Harold Berger Award, University of Pennsylvania, Spring 2009
- Tau Beta Pi membership, Fall 2007
- Eta Kappa Nu membership, Fall 2007
- National Science Foundation LS/AMP Research Fellowship, Summer 2007

## PUBLICATIONS AND PATENTS

### DISSERTATIONS

- **Daniel Lustig**, "Specifying, Verifying, and Translating Between Memory Consistency Models", *Ph.D. Dissertation, Princeton University*, November 2015.

### CONFERENCE PROCEEDINGS (REFEREED)

- **Daniel Lustig***, Geet Sethi*, Margaret Martonosi, and Abhishek Bhattacharjee, "COATCheck: Verifying Memory Ordering at the Hardware-OS Interface", *21st International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS),* Atlanta, GA, April 2016. Acceptance rate: 53/232=23%. (*: joint first authors)

- Yatin Manerkar, **Daniel Lustig**, Michael Pellauer, and Margaret Martonosi, "CCICheck: Using μhb Graphs to Verify the Coherence-Consistency Interface", *48th International Symposium on Microarchitecture (MICRO)*, Waikiki, HI, December 2015. Acceptance rate: 61/283=22%. **One of three nominees for Best Paper.**

- **Daniel Lustig**, Caroline Trippel, Michael Pellauer, and Margaret Martonosi, "ArMOR: Defending Against Consistency Model Mismatches in Heterogeneous Architectures", *42nd International Symposium on Computer Architecture (ISCA)*, Portland, OR, June 2015. Acceptance rate: 58/305=19%.

- **Daniel Lustig**, Michael Pellauer, and Margaret Martonosi, "PipeCheck: Specifying and Verifying Microarchitectural Enforcement of Memory Consistency Models", *47th International Symposium on Microarchitecture (MICRO)*, Cambridge, UK, December 2014 (to appear). Acceptance rate: 53/273=19%. **One of five nominees for Best Paper.**

- Angshuman Parashar, Michael Pellauer, Michael Adler, Bushra Ahsan, Neal Crago, **Daniel Lustig**, Vladimir Pavlov, Antonia Zhai, Mohit Gambhir, Aamer Jaleel, Randy Allmon, Rachid Rayess, Stephen Maresh, and Joel Emer, "Triggered Instructions: A Control Paradigm for Spatially-Programmed Architectures", *40th International Symposium on Computer Architecture (ISCA)*, Tel Aviv, Israel, June 2013. Acceptance rate: 56/288=19%

- **Daniel Lustig**, Margaret Martonosi, "Reducing GPU Offload Latency via Fine-Grained CPU-GPU Synchronization", *19th International Symposium on High Performance Computer Architecture (HPCA)*, Shenzhen, China, Feb. 2013. Acceptance rate: 51/249=20%

- Abhishek Bhattacharjee, **Daniel Lustig**, and Margaret Martonosi, "Shared Last-Level TLBs for Chip Multiprocessors", *17th International Symposium on High Performance Computer Architecture (HPCA)*, San Antonio, TX, USA, Feb. 2011. Acceptance rate: 42/227=19%

**JOURNAL ARTICLES (REFEREED)**

- Michael Pellauer, Angshuman Parashar, Michael Adler, Bushra Ahsan, Randy Allmon, Neal Crago, Kermin Fleming, Mohit Gambhir, Aamer Jaleel, Tushar Krishna, **Daniel Lustig**, Stephen Maresh, Vladimir Pavlov, Rachid Rayess, Antonia Zhai, Joel Emer, "Efficient Control and Communication Paradigms for Coarse-Grained Spatial Architectures", ACM Transactions on Computer Systems (TOCS), 33(3), September 2015.

- **Daniel Lustig**, Michael Pellauer, and Margaret Martonosi. "Verifying Correct Microarchitectural Enforcement of Memory Consistency Models". *IEEE Micro*, 35 (3), May-June 2015. Issue: Top Picks from the Computer Architecture Conferences of 2014.

- Angshuman Parashar, Michael Pellauer, Michael Adler, Bushra Ahsan, Neal Crago, **Daniel Lustig**, Vladimir Pavlov, Antonia Zhai, Mohit Gambhir, Aamer Jaleel, Randy Allmon, Rachid Rayess, Stephen Maresh, and Joel Emer, "Efficient Spatial Processing Element Control via Triggered Instructions", *IEEE MICRO,* 34 (3), May-June 2014. Issue: Top Picks of the Computer Architecture Conferences of 2013.

- **Daniel Lustig**, Abhishek Bhattacharjee, and Margaret Martonosi, "TLB Improvements for Chip Multiprocessors: Inter-Core Cooperative Prefetchers and Shared Last-Level TLBs", *ACM Transactions on Architecture and Code Optimization (TACO)*, 10(1), April 2013.

- **Daniel Lustig**, "The Algebraic Independence of the Sum of Divisors Functions", *Journal of Number Theory*, 130 (11), 2010.

## PATENTS

- **Daniel Lustig**, Margaret Martonosi, "Fine-Grained CPU-GPU Synchronization Using Full/Empty Bits", pending (application filed Feb. 2013).

## PROFESSIONAL SERVICE

- External Reviewer, MICRO 2016
- Program Committee, IISWC 2016
- External Review Committee, PLDI 2016
- External Review Committee, ISCA 2016
- External Reviewer, HPCA 2014
- Reviewer, IEEE Computer Architecture Letters (CAL), 2013, 2015
- Reviewer, IEEE Micro, 2012, 2013

## TEACHING EXPERIENCE

Spring 2012 **Assistant in Instruction**, Princeton University
Advanced Computer Architecture (ELE/COS 475)
Course Instructor: David Wentzlaff

Spring 2009 **Teaching Assistant**, University of Pennsylvania
Microcontrollers and Embedded Systems (ESE 350)
Course Instructor: Lunal Khuon

Fall 2008 **Teaching Assistant**, University of Pennsylvania
Principles of Digital Design (ESE 201/202)
Course Instructor: Jan Van der Spiegel

Fall 2007 **Teaching Assistant**, University of Pennsylvania
Principles of Digital Design (ESE 201/202)
Course Instructor: Jan Van der Spiegel

## PROFESSIONAL MEMBERSHIPS

- Center for Future Architectures Research (C-FAR), part of STARnet/SRC (during Ph.D.)
- Gigascale Systems Research Center (GSRC), part of FCRP and SRC (during Ph.D.)
- ACM Student Member, ACM SIGARCH
- IEEE Student Member, IEEE TCCA
- Tau Beta Pi
- Eta Kappa Nu

(last updated in September 2016)