Daniel Lustig

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Education

- **Princeton University**
  Ph.D. in Electrical Engineering, November 2015
  M.A. in Electrical Engineering, September 2011
  Advisor: Margaret Martonosi
- **University of Pennsylvania**
  B.S.E., *summa cum laude*, May 2009

Professional Experience

- **NVIDIA**, Santa Clara, CA and Westford, MA
  Jul. 2022 – Present Principal Research Scientist, NVIDIA Research
  Oct. 2017 – Jun. 2022 Senior Research Scientist, NVIDIA Research
  Dec. 2015 – Sep. 2017 Research Scientist, NVIDIA Research

- **Princeton University**, Princeton, NJ
  Sep. 2009 – Nov. 2015 Graduate Student, Dept. of Electrical Engineering

- **Intel**, Hudson, MA
  Summer 2011, 2012, 2013 Graduate Technical Intern, VSSAD Group

- **Intel**, Hillsboro, OR
  Fall 2010 Graduate Technical Intern, Digital Enterprise Group

- **University of Pennsylvania**, Philadelphia, PA
  Jun. 2008 – Aug. 2009 Undergraduate Research Assistant

Awards and Honors

Paper Awards

- **Top Picks Honorable Mention**, "Mixed-Proxy Extensions for the NVIDIA PTX Memory Consistency Model", Daniel Lustig, Simon Cooksey, and Olivier Giroux, *IEEE Micro*, to appear.
- **Top Picks Honorable Mention**, "GPS: A Global Publish-Subscribe Model for Multi-GPU Memory Management", Harini Muthukrishnan, Daniel Lustig, David Nellans, and Thomas Wenisch, *IEEE Micro*, "Top Picks of the Computer Architecture Conferences of 2021", 42 (4), July-Aug 2022.
- **Best Paper Nomination**, "GPS: A Global Publish-Subscribe Model for Multi-GPU Memory Management, Harini Muthukrishnan, Daniel Lustig, David Nellans, and Thomas Wenisch, *54th International Symposium on Microarchitecture (MICRO)*, Virtual, October 2021.

- **Top Picks Honorable Mention**, "A Formal Analysis of the NVIDIA PTX Memory Consistency Model", Daniel Lustig, Sameer Sahasrabuddhe, and Olivier Giroux, *IEEE Micro*, 40 (3), "Top Picks of the Computer Architecture Conferences of 2019", 40 (3), May-June 2020.
- **Top Picks Selection**, "CheckMate: Automated Synthesis of Hardware Exploits and Security Litmus Tests", Caroline Trippel, Daniel Lustig, and Margaret Martonosi, *IEEE Micro*, 39 (3), "Top Picks of the Computer Architecture Conferences of 2018", May-June 2019.
- **Top Picks Honorable Mention**, "PipeProof: Automated Memory Consistency Proofs for Microarchitectural Specifications", Yatin A. Manerkar, Daniel Lustig, Margaret Martonosi, and Aarti Gupta, *IEEE Micro*, "Top Picks of the Computer Architecture Conferences of 2018", 39 (3), May-June 2019.
- **Best Paper Nomination**, "PipeProof: Automated Memory Consistency Proofs for Microarchitectural Specifications", Yatin A. Manerkar, Daniel Lustig, Margaret Martonosi, and Aarti Gupta, *51st International Symposium on Microarchitecture (MICRO)*, Fukuoka, Japan, October 2018.
- **Top Picks Selection**, "TriCheck: Memory Model Verification at the Trisection of Software, Hardware, and ISA", Caroline Trippel, Yatin A. Manerkar, Daniel Lustig, Michael Pellauer, and Margaret Martonosi, *IEEE Micro*, 38 (3), "Top Picks of the Computer Architecture Conferences of 2017", May-June 2018.
- **Top Picks Honorable Mention**, "RTLCheck: Verifying the Memory Consistency of RTL Designs", Yatin A. Manerkar, Daniel Lustig, and Margaret Martonosi, *IEEE Micro*, 38 (3), "Top Picks of the Computer Architecture Conferences of 2017", May-June 2018.
- **Top Picks Selection**, "COATCheck: Verifying Memory Ordering at the Hardware-OS Interface", Daniel Lustig, Geet Sethi, Abhishek Bhattacharjee, and Margaret Martonosi, *IEEE Micro*, 37 (3), "Top Picks of the Computer Architecture Conferences of 2016", May-June 2017.
- **Best Paper Nomination**, "CCICheck: Using μhb Graphs to Verify the Coherence-Consistency Interface", Yatin A. Manerkar, Daniel Lustig, Michael Pellauer, and Margaret Martonosi, *48th International Symposium on Microarchitecture (MICRO)*, Honolulu, HI, December 2015.
- **Top Picks Selection**, "PipeCheck: Specifying and Verifying Microarchitectural Enforcement of Memory Consistency Models", Daniel Lustig, Michael Pellauer, and Margaret Martonosi, *IEEE Micro*, 34 (3), "Top Picks of the Computer Architecture Conferences of 2014", May-June 2015.
- **Best Paper Nomination**, "PipeCheck: Specifying and Verifying Microarchitectural Enforcement of Memory Consistency Models", Daniel Lustig, Michael Pellauer, and Margaret Martonosi, *47th International Symposium on Microarchitecture (MICRO)*, Cambridge, UK, December 2014.
- **Top Picks Selection**, "Triggered Instructions: A Control Paradigm for Spatially-Programmed Architectures", Angshuman Parashar, Michael Pellauer, Michael Adler, Bushra Ahsan, Neal Crago, Daniel Lustig, Vladimir Pavlov, Antonia Zhai, Mohit Gambhir, Aamer Jaleel, Randy Allmon, Rachid Rayess, Stephen Maresh, and Joel Emer, *IEEE Micro*, 34 (3), "Top Picks of the Computer Architecture Conferences of 2013", May-June 2014.

Other Honors

- RISC-V Technical Contributor Award, December 2021
- Invited Keynote Speech at ISPASS 2021
- Inaugural RISC-V Foundation Board of Directors' Award, December 2018
- Best in Session at SRC TECHCON 2014
- Intel PhD Fellowship, Fall 2013 – Spring 2014
- Featured Inventor, Celebrate Princeton Invention 2012
- Francis Upton Fellowship, Princeton University, Fall 2009 – Present
- William L. Everitt Student Award of Excellence, University of Pennsylvania, Spring 2009
- Faculty Appreciation Award, University of Pennsylvania, Spring 2009
- Honorable Harold Berger Award, University of Pennsylvania, Spring 2009
- Tau Beta Pi membership, Fall 2007
- IEEE-HKN (Eta Kappa Nu), Fall 2007

- National Science Foundation LS/AMP Research Fellowship, Summer 2007

Publications

Textbooks

1. "Architectural and Operating System Support for Virtual Memory", Abhishek Bhattacharjee and **Daniel Lustig**, Synthesis Lectures in Computer Archiecture, Morgan & Claypool Publishers, September 2017.

Conference Proceedings (refereed)

2. "Parsimony: Enabling SIMD/Vector Programming in Standard Compiler Flows", Vijay Kandiah, **Daniel Lustig**, Oreste Villa, David Nellans, and Nikos Hardavellas, *21st International Symposium on Code Generation and Optimization (CGO)*, Montréal, Canada, Mar 2023. *Artifact Evaluation Results: Results Reproduced (1.1), Artifacts Available (1.1), Artifacts Evaluated and Reusable (1.1).*
3. "FinePack: Transparently Improving the Efficiency of Fine-Grained Transfers in Multi-GPU Systems", Harini Muthukrishnan, **Daniel Lustig**, Oreste Villa, Thomas Wenisch, and David Nellans, *29th International Symposium on High Performance Computer Architecture (HPCA)*, Montréal, Canada, Mar 2023.
4. "Mixed-Proxy Extensions for the NVIDIA PTX Memory Consistency Model", **Daniel Lustig**, Simon Cooksey, and Olivier Giroux, *49th International Symposium on Computer Architecture (ISCA), Industry Track*, New York, NY, June 2022. ***I***EEE Micro Top Picks Honorable Mention,
5. "GPS: A Global Publish-Subscribe Model for Multi-GPU Memory Management", Harini Muthukrishnan, **Daniel Lustig**, David Nellans, and Thomas Wenisch, *54th International Symposium on Microarchitecture (MICRO)*, Virtual, October 2021. ***O***ne of Four Nominees for Best Paper, and IEEE Micro Top Picks Honorable Mention,
6. "Efficient Multi-GPU Shared Memory via Automatic Optimization of Fine-grained Transfers", Harini Muthukrishnan, David Nellans, **Daniel Lustig**, Jeffrey A. Fessler, and Thomas Wenisch, *48th International Symposium on Computer Architecture (ISCA)*, Virtual, June 2021.
7. "Need for Speed: Experiences Building a Trustworthy GPU Simulator", Oreste Villa*, **Daniel Lustig***, Zi Yan*, Evgeny Bolotin, Yaosheng Fu, Niladresh Chatterjee, Nan Jiang, and David Nellans, *27th International Symposium on High Performance Computer Architecture (HPCA)*, Industry Track, Virtual, February 2021. (*: authors contributed equally)
8. "HMG: Extending Cache Coherence Protocols Across Modern Hierchical Multi-GPU Systems", Xiaowei Ren, **Daniel Lustig**, Evgeny Bolotin, Aamer Jaleel, Oreste Villa, and David Nellans, *26th International Symposium on High Performance Computer Architecture (HPCA)*, San Diego, CA, February 2020.
9. "Translation Ranger: Operating System Support for Contiguity-Aware TLBs", Zi Yan, **Daniel Lustig**, David Nellans, and Abhishek Bhattacharjee, *46th International Symposium on Computer Architecture (ISCA)*, Phoenix, AZ, June 2019.
10. "A Formal Analysis of the NVIDIA PTX Memory Consistency Model", **Daniel Lustig**, Sameer Sahasrabuddhe, and Olivier Giroux, *24th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Providence, RI, April 2019. ***IEEE Micro Top Picks Honorable Mention***
11. "Nimble Page Management for Tiered Memory Systems", Zi Yan, **Daniel Lustig**, David Nellans, and Abhishek Bhattacharjee, *24th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Providence, RI, April 2019.
12. "PipeProof: Automated Memory Consistency Proofs for Microarchitectural Specifications", Yatin A. Manerkar, **Daniel Lustig**, Margaret Martonosi, and Aarti Gupta, *51st International Symposium on*

Microarchitecture (MICRO), Fukuoka, Japan, October 2018. ***One of four nominees for Best Paper, and IEEE Micro Top Picks Honorable Mention.***

13. "CheckMate: Automated Synthesis of Hardware Exploits and Security Litmus Tests", Caroline Trippel, **Daniel Lustig**, and Margaret Martonosi, *51st International Symposium on Microarchitecture (MICRO)*, Fukuoka, Japan, October 2018. ***IEEE Micro Top Pick, and shortlisted and invited to the Top Picks in Hardware and Embedded Security Workshop, Co-located with the 2022 International Conference On Computer Aided Design (ICCAD 2022).***
14. "RTLCheck: Verifying the Memory Consistency of RTL Designs", Yatin A. Manerkar, **Daniel Lustig**, and Margaret Martonosi, *50th International Symposium on Microarchitecture (MICRO)*, Cambridge, MA, October 2017. ***IEEE Micro Top Picks Honorable Mention***
15. "Automatic Synthesis of Comprehensive Memory Model Litmus Test Suites", **Daniel Lustig**, Andrew Wright, Alexandros Papakonstantinou, and Olivier Giroux, *22nd International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Xi'an, China, April 2017.
16. "TriCheck: Memory Model Verification at the Trisection of Software, Hardware, and ISA", Caroline Trippel, Yatin A. Manerkar, **Daniel Lustig**, Michael Pellauer, and Margaret Martonosi, *22nd International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Xi'an, China, April 2017. ***IEEE Micro Top Pick***
17. "COATCheck: Verifying Memory Ordering at the Hardware-OS Interface", **Daniel Lustig***, Geet Sethi*, Margaret Martonosi, and Abhishek Bhattacharjee, *21st International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Atlanta, GA, April 2016. (*: authors contributed equally) ***IEEE Micro Top Pick***
18. "CCICheck: Using μhb Graphs to Verify the Coherence-Consistency Interface", Yatin A. Manerkar, **Daniel Lustig**, Michael Pellauer, and Margaret Martonosi, *48th International Symposium on Microarchitecture (MICRO)*, Honolulu, HI, December 2015. ***One of three nominees for Best Paper***
19. "ArMOR: Defending Against Consistency Model Mismatches in Heterogeneous Architectures", **Daniel Lustig**, Caroline Trippel, Michael Pellauer, and Margaret Martonosi, *42nd International Symposium on Computer Architecture (ISCA)*, Portland, OR, June 2015.
20. "PipeCheck: Specifying and Verifying Microarchitectural Enforcement of Memory Consistency Models", **Daniel Lustig**, Michael Pellauer, and Margaret Martonosi, *47th International Symposium on Microarchitecture (MICRO)*, Cambridge, UK, December 2014. ***One of five nominees for Best Paper, and IEEE Micro Top Pick***
21. "Triggered Instructions: A Control Paradigm for Spatially-Programmed Architectures", Angshuman Parashar, Michael Pellauer, Michael Adler, Bushra Ahsan, Neal Crago, **Daniel Lustig**, Vladimir Pavlov, Antonia Zhai, Mohit Gambhir, Aamer Jaleel, Randy Allmon, Rachid Rayess, Stephen Maresh, and Joel Emer, *40th International Symposium on Computer Architecture (ISCA)*, Tel Aviv, Israel, June 2013. ***IEEE Micro Top Pick***
22. "Reducing GPU Offload Latency via Fine-Grained CPU-GPU Synchronization", **Daniel Lustig**, Margaret Martonosi, *19th International Symposium on High Performance Computer Architecture (HPCA)*, Shenzhen, China, February 2013.
23. "Shared Last-Level TLBs for Chip Multiprocessors", Abhishek Bhattacharjee, **Daniel Lustig**, and Margaret Martonosi, *17th International Symposium on High Performance Computer Architecture (HPCA)*, San Antonio, TX, USA, February 2011.

Journal Articles (refereed)

24. "Security Verification Through Automatic Hardware-Aware Exploit Synthesis: the CheckMate Approach", Caroline Trippel, **Daniel Lustig**, and Margaret Martonosi, *IEEE Micro*, 39 (3), May-June 2019. Issue: Top Picks from the Computer Architecture Conferences of 2018.
25. "Full-Stack Memory Model Verification with TriCheck", Caroline Trippel, Yatin A. Manerkar, **Daniel Lustig**, Michael Pellauer, and Margaret Martonosi, *IEEE Micro*, 38 (3), May-June 2018. Issue: Top

Picks from the Computer Architecture Conferences of 2017.

26. "Transistency Models: Memory Ordering at the Hardware-OS Interface", **Daniel Lustig**, Geet Sethi, Abhishek Bhattacharjee, and Margaret Martonosi, *IEEE Micro*, 37 (3), May-June 2017. Issue: Top Picks from the Computer Architecture Conferences of 2016.
27. "Efficient Control and Communication Paradigms for Coarse-Grained Spatial Architectures", Michael Pellauer, Angshuman Parashar, Michael Adler, Bushra Ahsan, Randy Allmon, Neal Crago, Kermin Fleming, Mohit Gambhir, Aamer Jaleel, Tushar Krishna, **Daniel Lustig**, Stephen Maresh, Vladimir Pavlov, Rachid Rayess, Antonia Zhai, Joel Emer, *ACM Transactions on Computer Systems (TOCS)*, 33(3), September 2015.
28. "Verifying Correct Microarchitectural Enforcement of Memory Consistency Models". **Daniel Lustig**, Michael Pellauer, and Margaret Martonosi, *IEEE Micro*, 35 (3), May-June 2015. Issue: Top Picks from the Computer Architecture Conferences of 2014.
29. "Efficient Spatial Processing Element Control via Triggered Instructions", Angshuman Parashar, Michael Pellauer, Michael Adler, Bushra Ahsan, Neal Crago, **Daniel Lustig**, Vladimir Pavlov, Antonia Zhai, Mohit Gambhir, Aamer Jaleel, Randy Allmon, Rachid Rayess, Stephen Maresh, and Joel Emer, *IEEE Micro*, 34 (3), May-June 2014. Issue: Top Picks from the Computer Architecture Conferences of 2013.
30. "TLB Improvements for Chip Multiprocessors: Inter-Core Cooperative Prefetchers and Shared Last-Level TLBs", **Daniel Lustig**, Abhishek Bhattacharjee, and Margaret Martonosi, *ACM Transactions on Architecture and Code Optimization (TACO)*, 10(1), April 2013.
31. "The Algebraic Independence of the Sum of Divisors Functions", **Daniel Lustig**, *Journal of Number Theory*, 130 (11), 2010.

Dissertations

32. "Specifying, Verifying, and Translating Between Memory Consistency Models", **Daniel Lustig**, *Ph.D. Dissertation, Princeton University*, November 2015.

Preprints and Standards Body Papers (non-refereed)

33. "P2535R0: Message fences", **Daniel Lustig**, Olivier Giroux, ISO JTC1/SC22/WG21, the C++ Standards Committee, latest revision February 2022
34. "P0668R5: Revising the C++ memory model", Hans-J. Boehm, Olivier Giroux, Viktor Vafeiadis, with input from from Will Deacon, Doug Lea, **Daniel Lustig**, Paul McKenney and others, ISO JTC1/SC22/WG21, the C++ Standards Committee, latest revision November 2018
35. "RealityCheck: Bringing Modularity, Hierarchy, and Abstraction to Automated Microarchitectural Memory Consistency Verification", Yatin A. Manerkar, **Daniel Lustig**, Margaret Martonosi, `arXiv:2003.04892 [cs.DC]`, March 2020.
36. "P0668R5: Revising the C++ memory model", Hans-J. Boehm, Olivier Giroux, Viktor Vafeiadis, with input from from Will Deacon, Doug Lea, **Daniel Lustig**, Paul McKenney and others, ISO JTC1/SC22/WG21, the C++ Standards Committee, latest revision November 2018
37. "P1239R0: Placed Before", **Daniel Lustig**, ISO JTC1/SC22/WG21, the C++ Standards Committee, latest revision October 2018
38. Chapter "RVWMO Memory Consistency Model, Version 0.1" and Appendix "RVWMO Explanatory Material, Version 0.1" of the *RISC-V Instruction Set Manual, Volume I: Unprivileged ISA* (with help from many other members of the RISC-V Memory Model task group), May 2018.
39. "MeltdownPrime and SpectrePrime: Automatically-Synthesized Attacks Exploiting Invalidation-Based Coherence Protocols", Caroline Trippel, **Daniel Lustig**, and Margaret Martonosi, `arXiv:1802.03802 [cs.CR]`, February 2018.
40. "Weak Memory Models with Matching Axiomatic and Operational Definitions", Sizhuo Zhang, Muralidaran Vijayaraghavan, **Daniel Lustig**, Arvind, `arXiv:1710.04259 [cs.PL]`, October 2017.

41. "Counterexamples and Proof Loophole for the C/C++ to POWER and ARMv7 Trailing-Sync Compiler Mappings", Yatin A. Manerkar, Caroline Trippel, **Daniel Lustig**, Michael Pellauer, and Margaret Martonosi, `arXiv:1611.01507 [cs.PL]`, November 2016.
42. "TriCheck: Memory Model Verification at the Trisection of Software, Hardware, and ISA", Caroline Trippel, Yatin A. Manerkar, **Daniel Lustig**, Michael Pellauer, Margaret Martonosi, `arXiv:1608.07547 [cs.AR]`, August 2016.

Professional Service

Technical Program Committee Leadership

- Chair, Technical Program Committee: International Symposium on High Performance Computer Architecture (HPCA), Industry Track: 2022

Technical Program Committee Membership

- Member, Technical Program Committee: International Symposium on Computer Architecture (ISCA), Industry Track: 2022
- Member, Technical Program Committee: International Conference on Architectural Support or Programming Languages and Operating Systems (ASPLOS): 2021
- Member, Technical Program Committee: International Symposium on High Performance Computer Architecture (HPCA), Industry Track: 2021
- Member, Technical Program Committee: International Symposium on Computer Architecture (ISCA): 2020, 2023
- Member, Technical Program Committee: International Symposium on Microarchitecture (MICRO): 2018
- Member, Technical Program Committee: International Symposium on Workload Characterization (IISWC): 2016, 2017
- Member, External Review Committee: International Conference on Architectural Support or Programming Languages and Operating Systems (ASPLOS): 2018, 2019
- Member, External Review Committee: International Symposium on High Performance Computer Architecture (HPCA): 2019
- Member, External Review Committee: International Symposium on Microarchitecture (MICRO): 2016, 2019, 2021
- Member, External Review Committee: International Symposium on Computer Architecture (ISCA): 2014, 2017
- Member, External Review Committee: International Conference on Programming Language Design and Implementation (PLDI): 2016

Journal Reviews

- Reviewer: IEEE Micro: 2012, 2013, 2017, 2018, 2019
- Reviewer: IEEE CAL, 2013, 2015

Funding Panels

- National Science Foundation: 2022

Student Mentoring Workshops

- 2021 7th Career Workshop for Inclusion and Diversity in Computer Architecture (CWIDCA), in conjunction with MICRO 2021, Virtual, October 2021
- 2021 Young Architect Workshop (YArch), in conjunction with ASPLOS 2021, Virtual, April 2021
- 2018 CRA-W Cross-layer Computing Summer School: Circuits, Architecture, and Systems, Evanston, IL, August 2018
- 2018 CRA Grad Cohort Workshop for Underrepresented Minorities and Persons with Disabilities (URMD), San Diego, CA, March 2018
- Second Career Workshop for Women and Minorities in Computer Architecture (CWWMCA), in conjunction with MICRO 2015, Honolulu, HI, December 2015

Open-Source Projects

- Chair of the RISC-V Virtual Memory Task Group, 2020-2021 (completion)
- Member of the RISC-V Technical Steering Committee, 2019-2020
- Reviewer, Linux Kernel Memory Consistency Model (LKMM), 2018-present
- Chair of the RISC-V Memory Consistency Model Task Group, 2017-2019 (completion)

Talks

Invited Talks

1. Keynote Presentation, International Symposium on Performance Analysis of Systems and Software (ISPASS), Virtual, March 2021
2. "Panel Discussion and Training and Exercise Session: Getting Ready for Research", with Sule Ozev, Josiah Hester, Seda Memik, *CRA-W Cross-layer Computing Summer School: Circuits, Architecture, and Systems*, Evanston, IL, August 2018
3. "Panel Discussion: School Daze: Dealing with Advisers, Labmates, and Networking", with Daniel Jimenez, Carole-Jean Wu, and Russ Joseph, *CRA-W Cross-layer Computing Summer School: Circuits, Architecture, and Systems*, Evanston, IL, August 2018
4. "How Academic Research Helps Us Build a Better GPU", Research Talk, *CRA-W Cross-layer Computing Summer School: Circuits, Architecture, and Systems*, Evanston, IL, August 2018
5. "Ph.D. Non-Academic Career Paths and Job Search", with Alan Bivens, *CRA Grad Cohort Workshop for Underrepresented Minorities and Persons with Disabilities (URMD)*, San Diego, CA, March 2018
6. "Building Your Professional Persona", with Chad Jenkins, *CRA Grad Cohort Workshop for Underrepresented Minorities and Persons with Disabilities (URMD)*, San Diego, CA, March 2018
7. Discussion Panelist, with Krsté Asanovic, Yunsup Lee, and Andrew Waterman, *2nd Workshop on Computer Architecture Research with RISC-V (CARRV)*, in conjunction with ISCA, June 2018
8. "RISC-V Memory Consistency Model Task Group Update", 8th RISC-V Workshop, Barcelona, Spain, May 2018
9. "RISC-V Memory Consistency Model Status Update", 7th RISC-V Workshop, Milpitas, CA, December 2017
10. "Status of the RISC-V Memory Consistency Model", 6th RISC-V Workshop, Shanghai, China, May 2017
11. "Automatic Synthesis of Comprehensive Litmus Test Suites", Dagstuhl Seminar 16471, "Concurrency with Weak Memory Models: Semantics, Languages, Compilation, Verification, Static Analysis, and Synthesis", April 2017
12. "Checking microarchitectural implementations of weak memory", Microsoft Research, Cambridge, UK, December 2014

13. "Specifying and Verifying Microarchitectural Enforcement of Memory Consistency Models", with Margaret Martonosi, IBM Research, Yorktown Heights, December 2014

Conference Talks

14. "Mixed-Proxy Extensions for the NVIDIA PTX Memory Consistency Model", *49th International Symposium on Computer Architecture (ISCA)*, Industry Track, New York, NY, June 2022.
15. "Need for Speed: Experiences Building a Trustworthy GPU Simulator", Lightning Talk, *27th International Symposium on High Performance Computer Architecture (HPCA)*, Industry Track, Virtual, February 2021.
16. "A Formal Analysis of the NVIDIA PTX Memory Consistency Model", *24th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Providence, RI, April 2019.
17. "Automatic Synthesis of Comprehensive Memory Model Litmus Test Suites", *22nd International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Xi'an, China, April 2017.
18. "COATCheck: Verifying Memory Ordering at the Hardware-OS Interface", *21st International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Atlanta, GA, April 2016.
19. "ArMOR: Defending Against Consistency Model Mismatches in Heterogeneous Architectures", *42nd International Symposium on Computer Architecture (ISCA)*, Portland, OR, June 2015.
20. "PipeCheck: Specifying and Verifying Microarchitectural Enforcement of Memory Consistency Models", *47th International Symposium on Microarchitecture (MICRO)*, Cambridge, UK, December 2014.
21. "Reducing GPU Offload Latency via Fine-Grained CPU-GPU Synchronization", *19th International Symposium on High Performance Computer Architecture (HPCA)*, Shenzhen, China, February 2013.

Students Supervised

1. Vijay Kandiah, Northwestern University: Intern, Spring 2022
2. Ketaki Joshi, Yale University: Intern, Summer 2021
3. Harini Muthukrishnan, University of Michigan: Intern, Summer 2020
4. Yatin Manerkar, Princeton University: PhD Dissertation Committee
5. Caroline Trippel, Princeton University: PhD Dissertation Committee
6. Guilherme Cox, Rutgers University: PhD Dissertation Committee
7. Xiaowei Ren, University of British Columbia: Intern, Summer 2017 and Summer 2018
8. Simon Cooksey, University of Kent: Intern, Summer 2018

Software Releases

1. Artfact for "Parsimony: Enabling SIMD/Vector Programming in Standard Compiler Flows." `https://github.com/NVlabs/Parsimony-CGO23` and `https://doi.org/10.5281/zenodo.7524279`.
2. RISC-V Axiomatic Virtual Memory Model Formalization using z3py, used during the development of new virtual memory extensions to the RISC-V Privileged ISA Specification: `https://github.com/daniellustig/riscv_axiomatic`
3. NVIDIA PTX Axiomatic Memory Model Formalization in Alloy and associated Coq proofs, released in support of our ASPLOS 2019 paper: `https://github.com/NVlabs/ptxmemorymodel`
4. RISC-V Axiomatic Memory Model Formalization in Alloy, used during the development of RVWMO, which was adopted as the memory consistency model for RISC-V: `https://github.com/daniellustig/riscv-memory-model`

5. Automatic Synthesis of Comprehensive Memory Model Litmus Test Suites, tool developed in Alloy, released in support of our ASPLOS 2017 paper: `https://github.com/NVlabs/litmustestgen`
6. COATCheck: released in support of our ASPLOS 2016 paper: `https://github.com/daniellustig/coatcheck`
7. PipeCheck: released in support of our MICRO 2015 paper: `https://github.com/daniellustig/pipecheck`
8. ArMOR: released in support of our ISCA 2015 paper: `https://github.com/daniellustig/armor`

Popular Press

1. "Researchers Find New Ways to Exploit Meltdown and Spectre Vulnerabilities in Modern CPUs", Gizmodo, February 2018.
2. "Researchers discover new ways to abuse Meltdown and Spectre flaws", Engadget, February 2018.
3. "The RISC-V Memory Consistency Model", *riscv.org blog*, April 2017.
4. "Tool for checking complex computer architectures reveals flaws in emerging design", *Princeton University News Release*, April 2017.
5. "Tool checks computer architectures, reveals flaws in emerging design", phys.org, April 2017.